09 22 3046

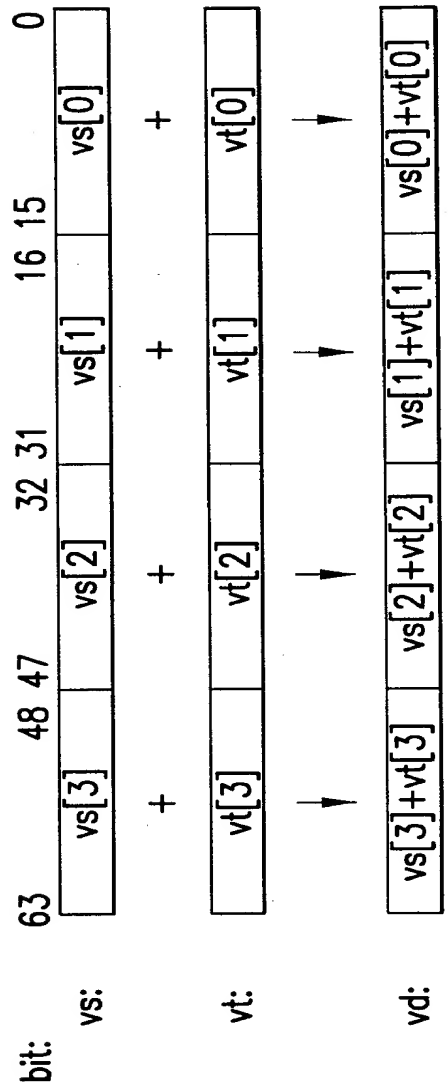

FIG.1
PRIOR ART

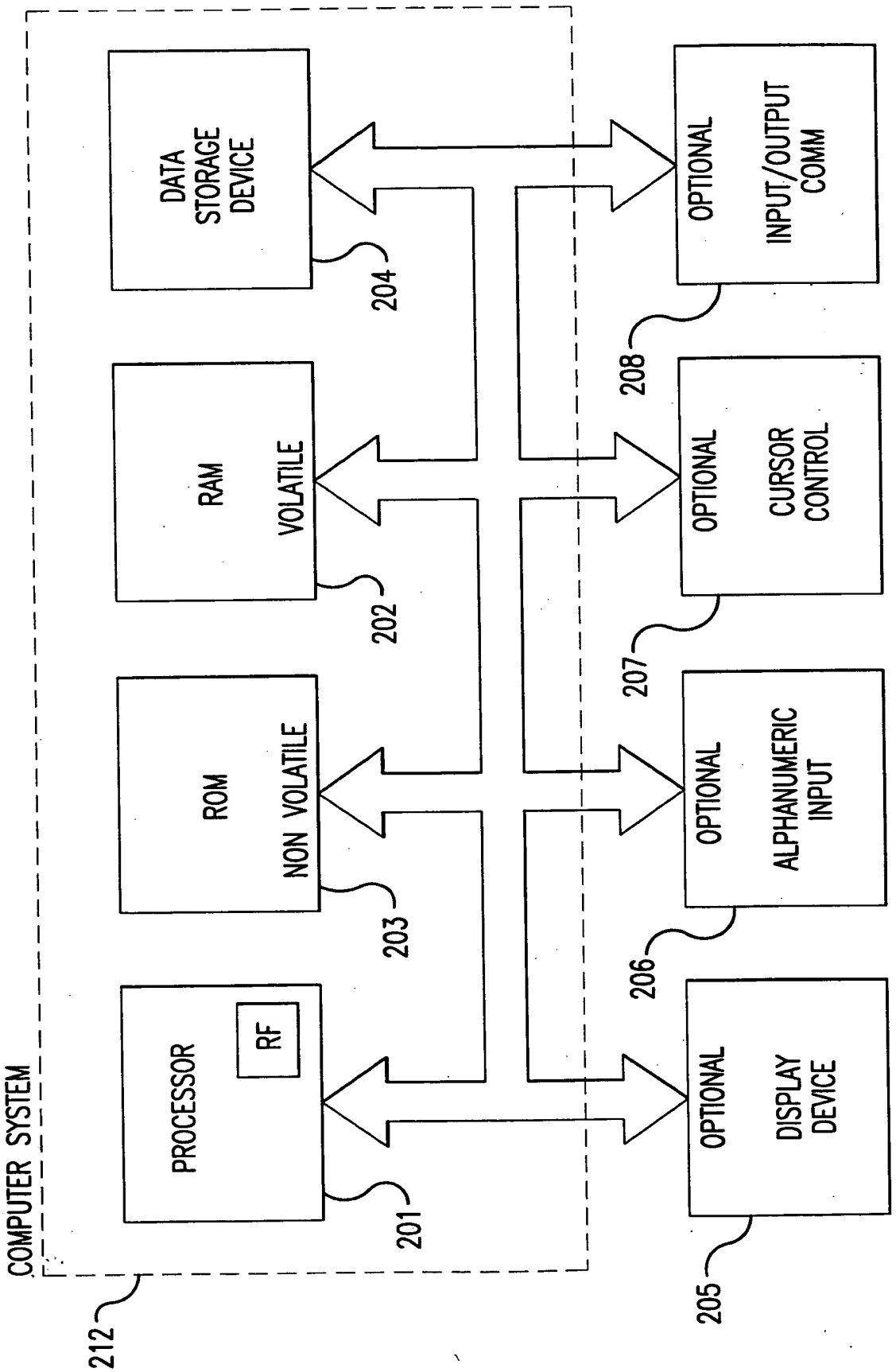
COMPUTER SYSTEM
212
PROCESSOR
RF
201
ROM
NON VOLATILE
203
RAM
VOLATILE
202
DATA
STORAGE
DEVICE
204
OPTIONAL
DISPLAY
DEVICE
205
OPTIONAL
ALPHANUMERIC
INPUT
206
OPTIONAL
CURSOR
CONTROL
207
OPTIONAL
INPUT/OUTPUT
COMM
208

FIG.2

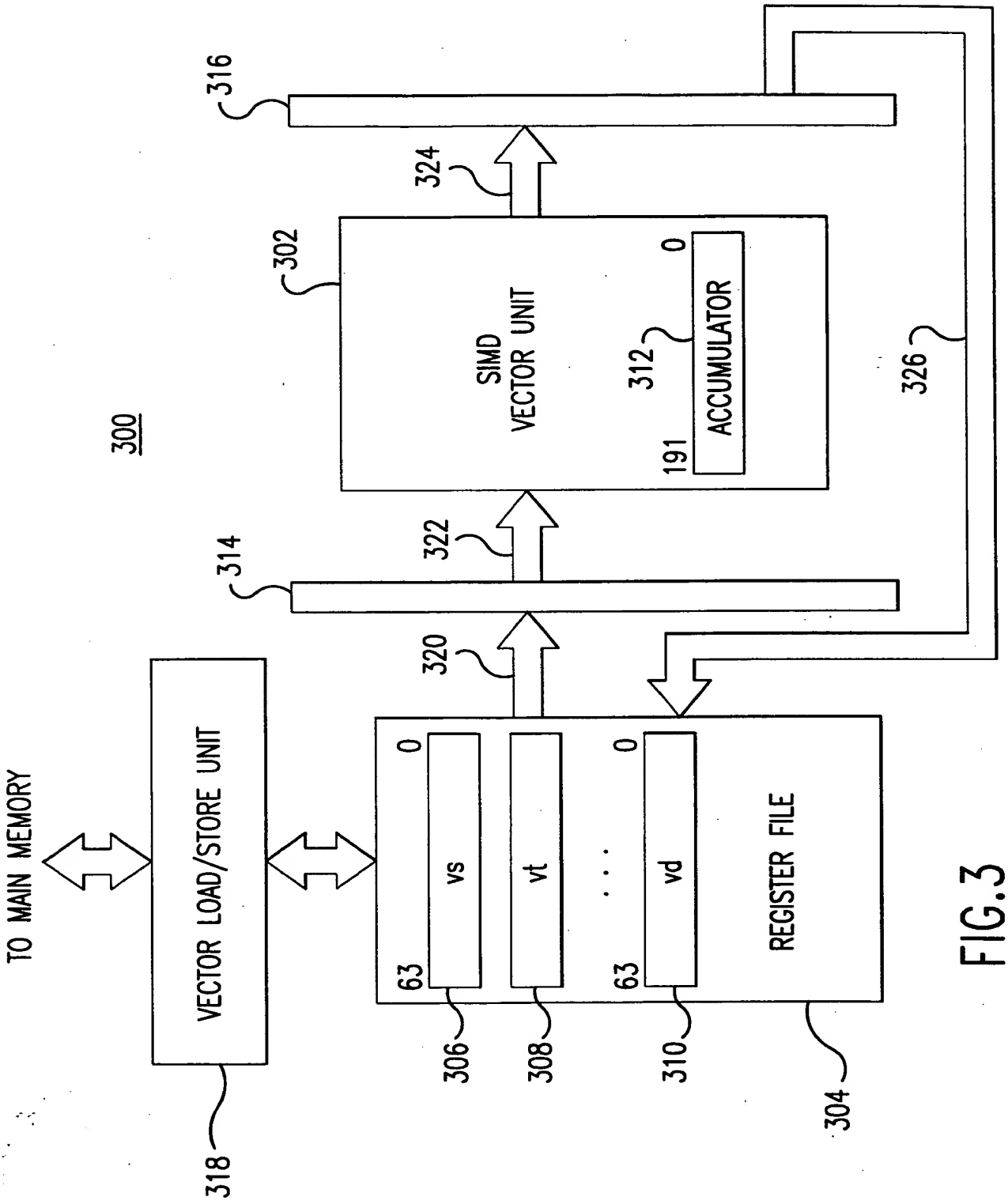
300
316
324
302
SIMD VECTOR UNIT
0
312
ACCUMULATOR
191
326
322
314
320
TO MAIN MEMORY
VECTOR LOAD/STORE UNIT
0
63
vs
vt
. . .
vd
REGISTER FILE
306
308
310
304
318

FIG.3

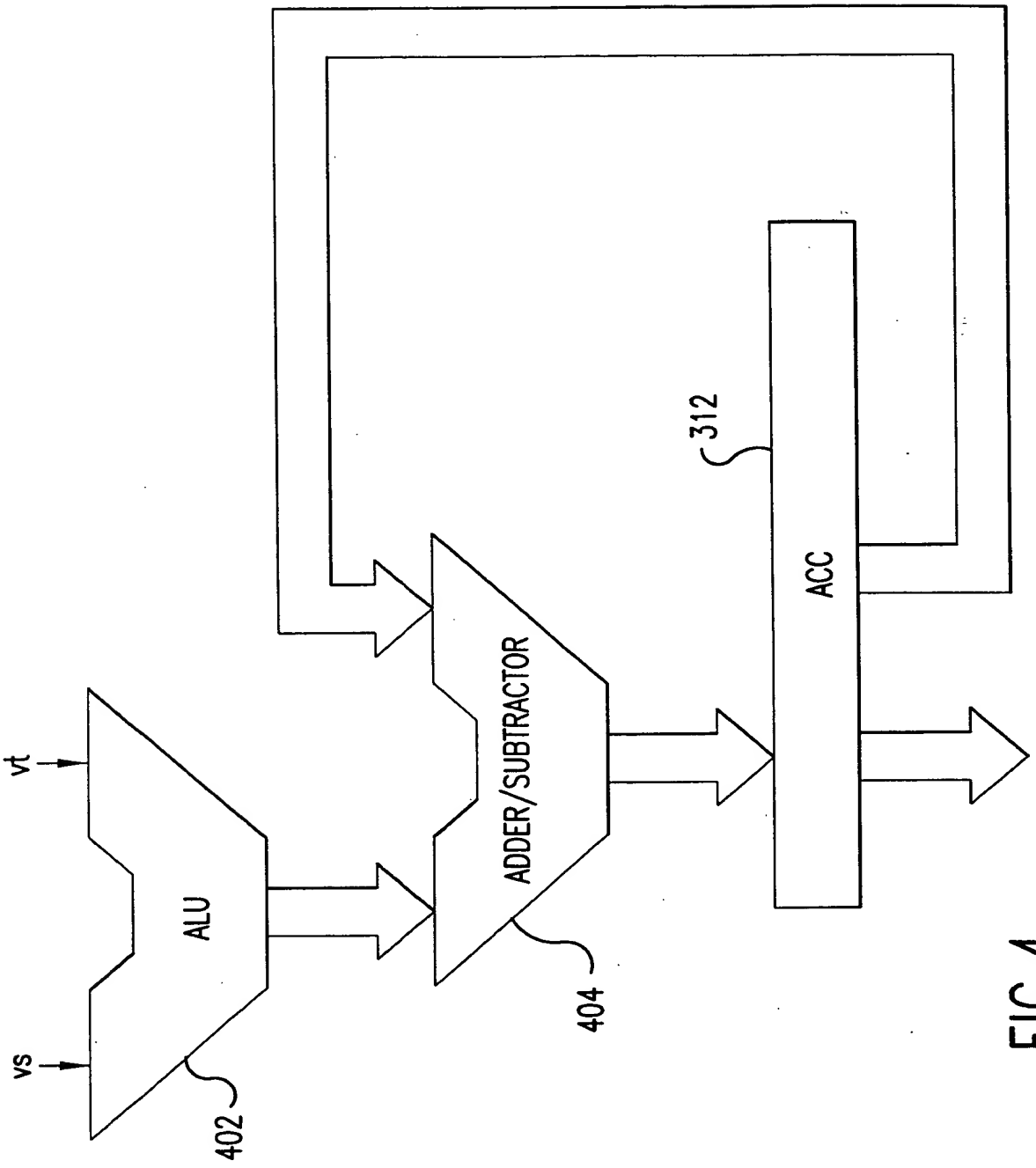

FIG.4

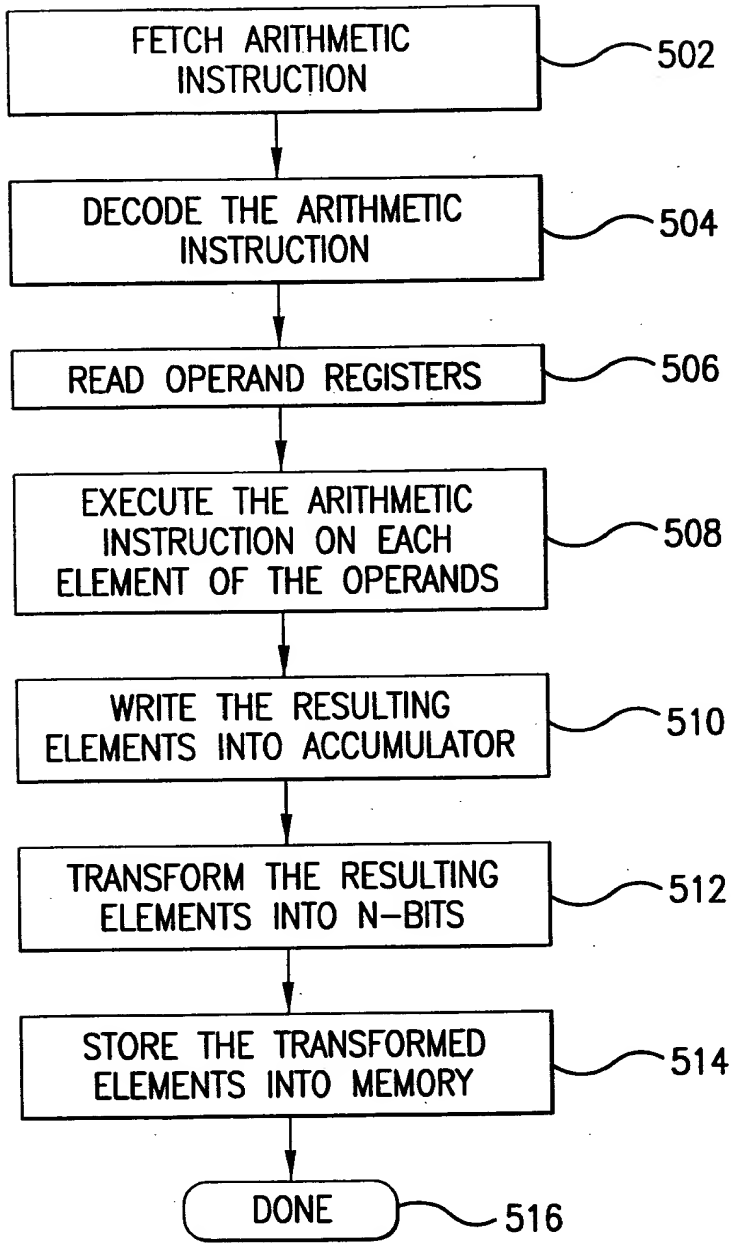
FETCH ARITHMETIC INSTRUCTION
502
DECODE THE ARITHMETIC INSTRUCTION
504
READ OPERAND REGISTERS
506
EXECUTE THE ARITHMETIC INSTRUCTION ON EACH ELEMENT OF THE OPERANDS
508
WRITE THE RESULTING ELEMENTS INTO ACCUMULATOR
510
TRANSFORM THE RESULTING ELEMENTS INTO N-BITS
512
STORE THE TRANSFORMED ELEMENTS INTO MEMORY
514
DONE
516

FIG.5

QH DATA TYPE ELEMENT SELECT FORMAT

	63 48	47 32	31 16	15 0	
vt:	D	C	B	A	600
	A	A	A	A	602
	B	B	B	B	604
	C	C	C	C	606
	D	D	D	D	608
	D	C	B	A	610

FIG.6

OB DATA TYPE ELEMENT SELECT FORMAT

	63 56	55 48	47 40	39 32	31 24	23 16	15 8	7 0	
vt:	H	G	F	E	D	C	B	A	700
	A	A	A	A	A	A	A	A	702
	B	B	B	B	B	B	B	B	704
	C	C	C	C	C	C	C	C	706
	D	D	D	D	D	D	D	D	708
	E	E	E	E	E	E	E	E	710
	F	F	F	F	F	F	F	F	712
	G	G	G	G	G	G	G	G	714
	H	H	H	H	H	H	H	H	716
	H	G	F	E	D	C	B	A	718

FIG.7

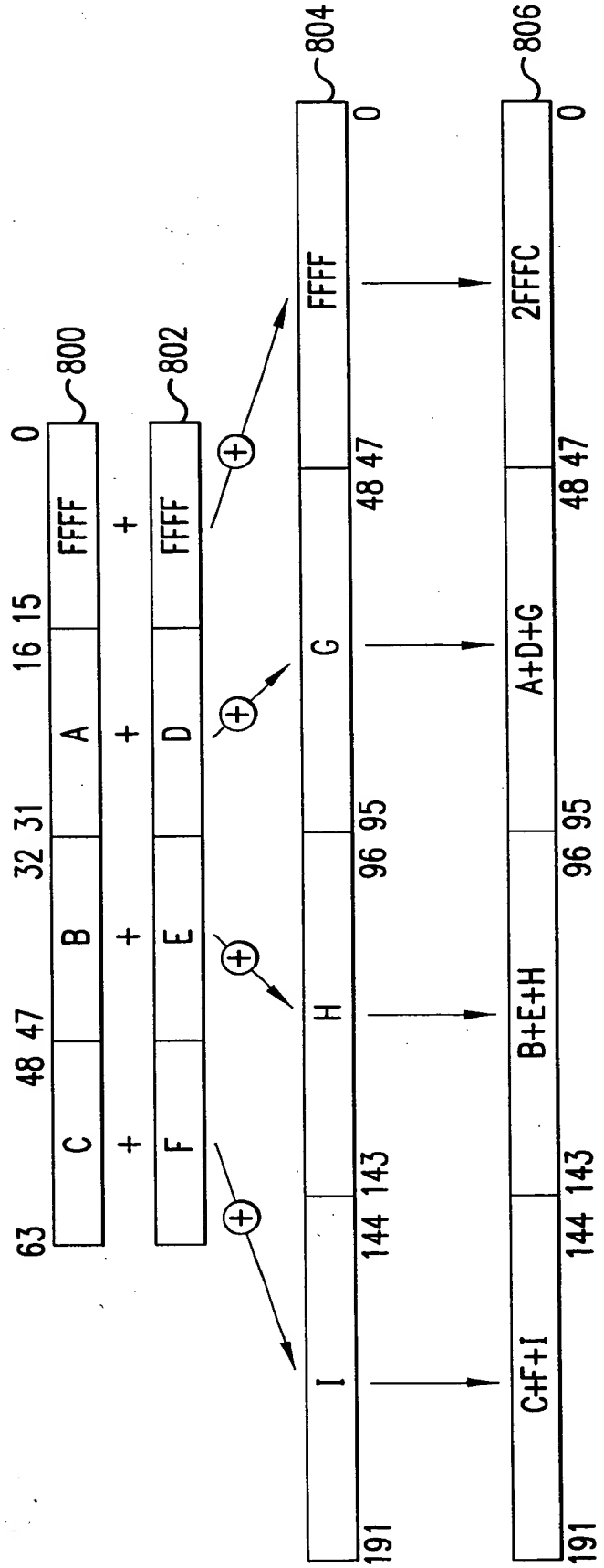
800
802
804
806
0
15
16
31
32
47
48
63
FFFF
A
B
C
FFFF
D
E
F
G
H
I
2FFFC
A+D+G
B+E+H
C+F+I
95
96
143
144
191
+

FIG.8

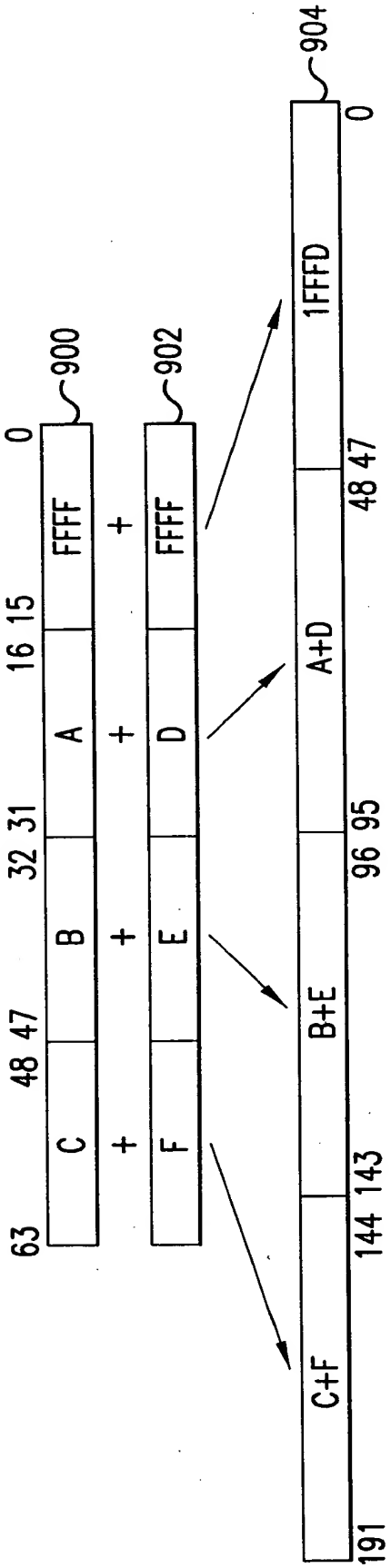
900
902
904
0
16 15
32 31
48 47
63
FFFF
A
B
C
FFFF
D
E
F
1FFFD
A+D
B+E
C+F
0
48 47
96 95
144 143
191
+
+
+

FIG.9